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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,004	07/31/2003	Inderjit Singh	NVIDP234/P000825	8949

28875 7590 03/17/2006

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EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,004	SINGH ET AL.	
	Examiner	Art Unit	
	Hung Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-18,20,21,27,29 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-18,20,21,27,29 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/17/05,01/23/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 2, 4-18, 20, 21, 27, 29 and 30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification does not disclose an entirety of at least one of the transistors is disposed directly below the bond pad, as recited in claim 1, 20 and 21.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4 – 18, 20, 27, 29 and 30, in so far as in compliance with 35 USC 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (PN 6,707,156, of record) in view of Tanaka (PN 6,100,589, of record).

Suzuki et al. discloses, as shown in Figure 1, an integrated circuit, comprising:

an active circuit (13);

a metal layer (M1L-M10L) disposed, at least partially, above the active circuit;

a bond pad (M11L) disposed, at least partially, above the metal layer;

wherein the metal layer is disposed, at least partially, directly above the active circuit;

wherein the metal layer ensures that bonds are capable of being placed over the active circuit and/or the at least one transistor;

wherein the active circuit includes a plurality of transistors, and an entirety of at least one of the transistors is disposed directly below the bond pad.

Suzuki et al. does not disclose the metal layer defines a mesh. However, Tanaka discloses an integrated circuit comprising a metal layer defined a mesh. Note Figures 1-12 of Tanaka. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the integrated circuit of Suzuki et al. having the metal layer defined a mesh, such as taught by Tanaka in order to further improve the mechanical strength and to further enhance the effects for suppressing crack formation in the insulation interlayer so that it inherently prevents the damage to the active circuit and/or the at least one transistor during the bonding process.

Regarding claim 4, Suzuki et al. and Tanaka disclose the metal layer includes an interconnect metal layer.

Regarding claim 5, Suzuki et al. and Tanaka disclose the interconnect metal layer interconnects the bond pad with a plurality of underlying metal layers.

Regarding claim 6, Suzuki et al. and Tanaka disclose each of the underlying metal layers is in electrical communication by way of a plurality of vias (110a-c and 120a-c).

Regarding claim 7, Suzuki et al. and Tanaka disclose the metal layer includes a plurality of openings (130a-i, 133a-i).

Regarding claim 8, it is inherent that the openings of Suzuki et al. and Tanaka are adapted for facilitating an interlock between the metal layer and an inter-metal dielectric layer disposed between the metal layer and the bond pad.

Regarding claim 9, Suzuki et al. and Tanaka disclose the inter-metal dielectric layer is constructed from a material selected from the group consisting of a low-K dielectric material [Col. 6, lines 35-44].

Regarding claim 10, Suzuki et al. and Tanaka disclose the openings are completely enclosed around a periphery thereof.

Regarding claim 11, Suzuki et al. and Tanaka disclose the openings have a substantially square configuration.

Regarding claim 12, Suzuki et al. and Tanaka disclose the openings define a plurality of substantially linear first portions and a plurality of substantially linear second portions which intersect.

Regarding claim 13, Suzuki et al. and Tanaka disclose the openings define a matrix of openings.

Regarding claim 14, Suzuki et al. and Tanaka disclose a plurality of interconnect vias are formed in rows along the first portions

Regarding claim 15, Suzuki et al. and Tanaka disclose the interconnect vias are spaced along a length of the first portions.

Regarding claim 16, Suzuki et al. and Tanaka disclose the interconnect vias include one single row for each of the first portions.

Regarding claim 17, Suzuki et al. and Tanaka disclose the interconnect vias include at least two spaced rows for each of the first portions.

Regarding claim 18, Suzuki et al. and Tanaka disclose a width of the fist portions is enlarged to accommodate the at least two spaced rows for each of the first portions.

Regarding claim 20, Suzuki et al. discloses, as shown in Figure 1, an integrated circuit, comprising:

an active circuit means (13) for processing electrical signals;

a metal layer (M1L-M10L) disposed, at least partially, above the active circuit means and including a metal layer means for preventing damage incurred during a bonding process;

a bond pad (M11L) disposed, at least partially, above the metal layer;

wherein the metal layer is disposed, at least partially, directly above the active circuit means;

wherein the metal layer ensures that bonds are capable of being placed over the active circuit means and/or the at least one transistor;

wherein the active circuit means includes a plurality of transistors, and an entirety of at least one of the transistors is disposed directly below the bond pad.

Suzuki et al. does not disclose the metal layer defines a mesh. However, Tanaka discloses an integrated circuit comprising a metal layer (200, 300) defined a mesh. Note Figures 1-22 of Tanaka. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the integrated circuit of Suzuki et al. having the metal layer defined a mesh, such as taught by Tanaka in order to further improve the mechanical strength and to further enhance the effects for suppressing crack formation in the insulation interlayer so that it inherently prevents the damage to the active circuit and/or the at least one transistor during the bonding process.

Regarding claim 27, Suzuki et al. and Tanaka disclose the metal layer is disposed, at least partially, above the active circuit along a vertical axis.

Regarding claim 29, Suzuki et al. and Tanaka disclose the inter-metal dielectric layer is constructed from a low-K dielectric material (polyimide and FSG). Note Figure 1, Col. 1, lines 39-51 and Col. 7, lines 26-38 of Suzuki et al..

Regarding claim 30, Suzuki et al. and Tanaka disclose the inter-metal dielectric layer is fluorinated silica glass (FSG) material. Note Figure 1, Col. 1, lines 39-51 and Col. 7, lines 26-38 of Suzuki et al..

3. Claims 2 and 21, in so far as in compliance with 35 USC 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (PN 6,707,156, of record) in view of Tanaka (PN 6,100,589, of record) and further in view of Applicants' Admitted Prior Art of Figures 1-2.

Suzuki et al. and Tanaka disclose the claimed invention including the integrated circuit as explained in the rejection above. Suzuki et al. and Tanaka does not disclose the active circuit including an input/output bus and a plurality of vertically spaced underlying metal layers, at least partially, under the active circuit. However, Applicants' Admitted Prior Art of Figures 1-2 disclose an active circuit including an input/output bus and a plurality of vertically spaced underlying metal layers (M1-M4), at least partially, under the active circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Suzuki et al. and Tanaka having the active circuit including an input/output bus and

a plurality of vertically spaced underlying metal layers, at least partially, under the active circuit, such as taught by Applicants' Admitted Prior Art of Figures 1-2 in order to provide the interconnects between the device and the external connection, and to integrate the multi-layer interconnect structures to perform a plurality of functions.

Response to Arguments

4. Applicant's arguments filed 01/05/06 have been fully considered but they are not persuasive.

It is argued, at page 8 of the Remarks, that none of the references relied upon suggest an entirety of at least one of the transistors being disposed directly below the bond pad and a mesh that ensures that at least one of the bonds is capable of being placed over the at least one transistor without damage thereto during the bonding process. This argument is not convincing because Suzuki et al. discloses, as shown in Figure 1, a metal layer (M1l-M10L) and an entirety of at least one of the transistors (13) being disposed directly below the bond pad (M11L). Suzuki et al. does not disclose the metal layer is a mesh. Tanaka, on the other hand, discloses a meshed metal layer (200,300) is used improve the mechanical strength and to further enhance the effects for suppressing crack formation in the insulation interlayer. Therefore, it inherently prevents the damage to the active circuit and/or the at least one transistor.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Tuesday to Friday 6:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272 - 1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vu

March 8, 2006

Hung Vu

Primary Examiner